Claims

[c1] What is claimed is:

1.A method of changing the audible volume level of a digital signal comprising:

providing a destination volume value to a DSP; and

with the DSP, gradually incrementing the volume level of the digital signal to the destination volume value within a predetermined time period;

whereby any destinationvolume designated by the destination volume value is achieved in the digital signal in the same amount of time.

[c2] 2.The method of claim 1 wherein the incrementing step further comprises:

gradually incrementing the digital signal within a predetermined sample number corresponding to the predetermined time period.

[c3] 3.The method of claim 2 wherein the incrementing step further comprises:

subtracting the current volume value of the digital signal from the destination volume value;

dividing the result from the subtracting step by the predetermined sample number to obtain a volume step;

incrementing the output signal by the volume step in a continuous fashion until the volume destination is reached.

[c4] 4.The method of claim 3 wherein the result from the subtracting step is a positive number.

[c5] 5.The method of claim 3 wherein the result from the subtracting step is a negative number.

[c6] 6.The method of claim 2 wherein the predetermined sample number is user-selectable.

[c7] 7.A Digital Signal Processor (DSP) for adjusting the volume of a digital signal stored in a data stream, the DSP comprising:
a processing unit for processing the data stream;
a first memory coupled to the processing unit for storing a destination volume value; and
a second memory coupled to the processing unit for storing a time_determining value;
wherein the processing unit adjusts the volume of the signal stored in the data stream according to the time_determining value such that the adjustment from a current volume value of the signal to the destination volume value is accomplished within a predetermined time.

[c8] 8.The DSP in claim 7 further comprising a program

memory coupled to the processing unit for storing a program controlling the flow of operations in the DSP.

[c9] 9.The DSP in claim 8 wherein the program memory comprises a ROM type memory.

[c10] 10.The DSP in claim 7 wherein the first memory comprises a register.

[c11] 11.The DSP in claim 7 wherein the second memory comprises a register.

[c12] 12. The DSP in claim 7 further comprising a data memory for storing temporary variables.

[c13] 13.The DSP in claim 12 wherein the data memory comprises an SRAM type memory.

[c14] 14.The DSP in claim 7 wherein the second memory stores a sample number corresponding to the predetermined time.